APPARATUS AND METHOD FOR BUS POWER
MEASUREMENT IN A DIGITAL SIGNAL PROCESSOR

This application claims the benefit of U.S. Provisional Application No.

5   60/299,016, filed June 18, 2001; and U.S. Provisional Application No. 60/299,023, filed

June 18, 2001.

Related U.S. Patent Application

10   U.S. Patent Application (Attorney Docket TI-33148), entitled APPARATUS

AND METHOD FOR CENTRAL PROCESSING UNIT POWER MEASUREMENT IN

A DIGITAL SIGNAL PROCESSOR, invented by Gary L. Swoboda, filed on even date

herewith, and assigned to the assignee of the present application is a related application.

15   **Background of the Invention**

1. Field of the Invention

This invention relates generally to digital signal processing units and, more

20   particularly, to power consumption of the buses found in digital signal processor units.

2. Background of the Invention

The digital signal processor and related devices have found increasing application

25   in portable apparatus, such as cell phones, wireless internet devices, etc. The power

consumption is a critical parameter for portable apparatus. The power consumption

determines the size of the battery and the time between recharging the battery, key

parameters in the portability of devices.

30   However, the power consumption parameter has several variables. The hardware

implementing the device can, for example, be designed to run with minimum power

expenditure. Even after every effort has been employed to reduce to power requirements of the implementing hardware, the software programs being executed by the hardware may not be optimized to provide minimum power consumption. In addition, not only can the central processing unit draw power, but bus activity can also result in the

5   consumption of power. However, before these parameters can be optimized, a technique for the measurement of the power consumption must be provided.

A need has therefore been felt for apparatus and an associated method having the feature that the power consumption in a digital signal processor unit can be measured. It

10   would be a feature of the apparatus and associated method to measure the power dissipated by the bus in a digital signal processing unit. It would be yet another feature of the apparatus and associated method to measure the power dissipated by the digital signal processor bus during a preselected period of activity. It would be a still further feature of the apparatus and associated method to separate the power consumed by internal bus and

15   the power consumed by the external bus in a digital signal processing unit. It would be yet another feature of the apparatus and associated method to determine the power consumption of a digital signal processor bus for a selected portion of a software program. It would be a still further feature of the present invention to determine separately the power consumption of a digital signal processor bus for a plurality of

20   portions of a software program.

Summary of the Invention

The aforementioned and other features are obtained, according to the present

25   invention, by measuring the number of transitions of the digital signal processing unit bus. The number of transition is determined by coupling a conducting lead to each conductor of digital signal processor bus. Each lead is coupled to an input terminal of a first latch/flip flop component. The output of the first latch/flip flop component is coupled a first terminal of a logic "exclusive OR" gate and to an input terminal of the

30   second latch/flip component. The output terminal of the second latch/flip flop component is coupled to a second input terminal of the logic "exclusive OR" gate. The

output terminal of the logic "exclusive OR" gate is coupled to a count unit, the count unit determining the number of transitions during each clock cycle. The count for each clock cycle is applied to an adder unit and the total number of counts determined. Because the transitions on all of the bus conductors are monitored, the total number of transitions

5   during a determined period can be determined. The total number of transitions determines the total energy consumption for a preselected period. The power consumed for an individual bus transition can be determined by simulation or by other techniques. The power consumed by the bus can be further divided into power consumed during the operation of the internal (on-chip) bus and the power consumed by the external (off-chip)

10   bus. The power consumed can also be separately determined for one or more portions of the software program.

Brief Description of the Drawings

15   Figure 1A is a block diagram of the apparatus for determining the number of bus logic signal transitions during a selected period according to the present invention, while Fig. 1B is a block diagram of an alternative implementation for determining the number of bus logic signal transitions according to the present invention.

20   Figure 2 is a block diagram illustrating the relationship of the internal (on-chip) bus and the external (off-chip) bus.

Description of the Preferred Embodiment

25   1. Detailed Description of the Figures

Referring to Fig. 1, a technique for measuring the power on a bus according to the present invention is illustrated. The signal on bus pin A of the bus is applied to latch/flip-flop 11A. The output terminal of latch/flip-flop 11A is applied to an input terminal of

30   latch/flip/flop 12A and to a first input terminal of logic exclusive "OR" gate 14A. The output terminal of the latch/flip-flop 12 is coupled to the second terminal of logic

"exclusive OR" gate **14A**. The output terminal of logic "exclusive OR" gate **14A** is coupled to an input terminal of count logic unit **15**. Similar apparatus couples bus pin **A+1** through bus pin **N** to the count logic unit **16**. The output of count logic unit **16** is applied to adder unit **16A** through adder unit **16Q**. The output signals of adder unit **16A** through **16Q** are applied to register/control devices **17A** through **17Q**, respectively. The output signals of the register/control devices **17A** through **17Q** are applied to adder units **16A** through **16Q** to be added to the count from count logic unit **15**. The output signals on the terminals of register/control devices **17A** through **17Q** are the total number of counted transitions. The register/control devices **17A** through **17Q** are activated by output signals from logic "AND" gates **19A** through **19Q**, respectively. Logic "AND" gates **19A** through **19Q** each have an input terminal that receives a control signal from trigger unit **18** and an input terminal that receives a LOAD signal to activate the apparatus. The trigger unit **18** receives control signals that can activate the counting of the internal bus transitions, the external bus transitions, and selected portions of the program. Therefore, bus transition counts can be simultaneously determined for the internal bus, the external bus, and selected portions of the program, i.e., each portion of the program typically being designated as a window.

Referring to Fig. 1B, an alternative implementation of the apparatus of Fig. 1A receiving signals from the count logic unit is shown. Adder unit **16A** and register/control device **17A** are coupled together and receive control signals as illustrated in Fig. 1A. However, rather than applying a total count number to the output terminal(s) of register/control device **17A**, the signal from the most significant bit of the internal register is applied to a first input terminal of logic "exclusive OR" gate **42A** and to an input terminal of latch/flip-flop **41A**. The latch/flip-flop **41A** delays the signal from the register/control unit **17A** for one clock cycle and applies the output signal to the second terminal of logic "exclusive OR" gate **42A**. The output signal from the logic "exclusive OR" gate is applied to an input terminal of counter unit **43A**. The result of this configuration is that the transition count can be scaled. A count is entered in the counter unit **43A** only when the register in register/control device **17A** has a logic "1" signal entered in the most significant bit position. Because of the speed of the modem

processor, this configuration can provide numerical transition counts of more manageable size. As will be clear the application to adder unit **16A** and register/control unit **17A** is exemplary and similar apparatus can be added to each of the adder unit **16X** and register/control unit **17X** pairs.

Referring to Fig. 2, the relationship of the internal or on-chip bus **24** to the external bus **25** is shown. The (on-chip) processor **21** is coupled to the internal bus **24**. The internal bus **24** is coupled to (on-chip) peripheral device **221** through (on-chip) peripheral device **22Q** and is coupled to buffer circuit **23**. Conducting leads are coupled to internal bus **24** to provide the signals bus pin A through bus pin N to the latch/flip-flop circuits shown in Fig. 1. The buffer circuit **23** is coupled to the external bus **25**. External bus **25** can be coupled to peripheral device **261** through peripheral device **26M** and can be coupled to one or more other chip (represented by chip **30**). Activity on the internal bus **24** is monitored by the signals on bus pin A through bus pin N. When the activity on (internal) bus **24** is directed to one of the devices coupled to external bus **25**, additional power must be provided to drive the additional capacitance of the components coupled to the external bus **25**. Buffer circuit **23** is part of the chip **20** configuration, the power used by the buffer circuit **23** is supplied by the power source (not shown) energizing chip **20**.

2. Operation of the Preferred Embodiment

Each logic signal transition on a bus conductor requires power. Therefore, by determining the number of transitions on the digital signal processor bus, the power consumed as a result of bus signal activity can be determined. The output signal of latch **12A** provides a one clock cycle delay as compared to the output signal of latch **11A**. Thus when a logic signal transition has occurred on the bus pin A, the "logic exclusive OR" gate will apply a signal indicating a logic signal transition to the count logic **15**. When no logic signal transition has occurred, no indication of a logic signal transition will be generated by the logic "exclusive OR" gate **14A**. Because the circuitry coupled bus pin A through bus pin N is similar, during each clock cycle, a signal will be applied to the count logic unit **15** for each bus pin experiencing a logic signal transition. The

count logic unit **15** determines the number of transitions that have occurred on the bus during the current clock cycle. The count from the count logic unit **15** is applied to adder unit **16**. The value in adder unit **16** is transferred to register/control device **17**. The register/control device **17** applies the contents of the register/control device **17** to output

5   terminals and to adder unit **16**. The contents of register/control device **17** can represent the total number of logic signal transitions. This value is returned to adder unit **16** so that subsequent transitions identified by adder unit **16** can be added thereto to form a cumulative total. Apparatus can be coupled to the register/control units to provide a scaled total transition count.

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    Because the number of transitions determines the power consumption resulting from bus usage, the total number of transitions provides the number from which the power consumption can be derived. The power consumed by each bus state transition can be determined by simulation techniques or by other techniques.

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    The trigger unit **18** can provide control signals that can activate and deactivate the register/control devices **17A** through **17Q**. These activations can occur during an identified external bus activity, during an internal bus activity, or both. Address signals can be used as control signals applied to trigger unit **18** distinguish between access to the

20   internal bus or access to the external bus. In addition, the trigger unit **18** can activate the register/control device **17A** (through **17Q**) during a preselected window or windows of operation. In Fig. 1B, when a plurality of register/control devices is available, a plurality of software program portions can be monitored.

25   While the invention has been described with respect to the embodiments set forth above, the invention is not necessarily limited to these embodiments. Accordingly, other embodiments, variations, and improvements not described herein are not necessarily excluded from the scope of the invention, the scope of the invention being defined by the following claims.

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